LISTING OF CLAIMS:

Claims 1-15 (Cancelled)

Claim 16 (Currently Amended) A MOSFET device ~~having~~ comprising a silicon substrate having shallow trench isolation STI located therein, ~~implanted wells,~~ a gate dielectric[[,]] and a ~~deposited and patterned~~ gate stack located on said silicon substrate, ~~implanted source/drain extensions, and a SiN etch stop layer deposited over the gate stack, the implanted wells and the implanted source/drain extensions, and an HDP oxide layer deposited primarily on horizontal surfaces over the SiN layer and over the gate stack, the implanted wells and the implanted source/drain extensions and used as protection from a fluorine implant to form~~ and a fluorine doped low K dielectric oxide gate ~~sidewall~~ spacers located on sidewalls of said gate stack, said fluorine doped low K dielectric oxide gate spacer having a fluorine content of about 1E14 to 2E16 cm^{-2} ~~such that low K properties of fluorine are used to develop a low parasitic capacitance MOSFET~~.

Claim 17 (Currently Amended) The MOSFET device of claim 16~~, having protection from a fluorine implant to form~~ wherein said fluorine doped low K dielectric oxide gate ~~sidewall~~ spacers~~, and having~~ has a dielectric constant value in ~~the~~ a range of 3.3 to 4.0.

Claim 18 (Currently Amended) The MOSFET device of claim 16~~, having protection from a fluorine implant to form~~ wherein said fluorine doped low K dielectric oxide gate ~~sidewall~~ spacers~~, and having~~ has a dielectric constant value of substantially 3.3.

Claim 19 (Cancelled)

Claim 20 (Currently Amended) The MOSFET device of claim 16~~, having protection from a fluorine implant to form fluorine doped low K dielectric oxide gate sidewall spacers, and~~ further ~~including~~ comprising a silicon nitride oxide layer located on at least said gate stack ~~formed over the MOSFET device~~.